Remarks

Applicant thanks the Examiner for the careful examination of this application and the clear explanation of the rejections.

The amended title better reflects the claimed matter.

The amended abstract includes the suggested changes.

Claims 1-24 and 30-36 are cancelled and may be presented for further prosecution in a divisional application.

Claims 25-29 are amended to "particularly point out and distinctly claim the subject matter the applicant regards as his invention." New claims 37-42 "particularly point out and distinctly claim the subject matter the applicant regards as his invention."

New claim 37 defines a process of reading words of data from a memory.

The process loads a control register with control data to select a memory access controller.

The process transfers a word of data in parallel from the memory into a data register in response to first control signals in a first state.

The process shifts data from the data register in series in response to first control signals in a second state.

The process transfers a word of data in parallel from the memory into the data register after the last data bit of the previous word of data is shifted out of the data register in response to memory access control signals from the memory access controller while maintaining the first control signals in the second state.

The process shifts data from the data register in series in response to memory access control signals from the memory access controller while maintaining the first control signals in the second state.

In contrast, US 4,346,440 to Kyu discloses A bit-oriented data link controller providing the interface between a microcomputer or terminal and a data communications link. The data link controller is capable of accommodating the three most commonly available bit-oriented data link control protocols, namely SDLC, HDLC, and ADCCP. The data link controller provides the data communications interface for both primary and secondary stations in stand-alone, polling, and loop configurations. The Kyu patent depicts a block diagram, Figure 8, illustrating the primary components of the ADLC. The Kyu patent also discloses several control and status register signals and protocol bits.

The Kyu patent fails to teach or disclose the specific claimed steps in claim 37 of loading a control register with control data to select a memory access controller, transferring and shifting a word of data in response to first control signals in respective first and second states, and transferring and shifting a word of data in response to memory access control signals while maintaining the first control signals in the second state.

US 4,768,190 to Giancarlo discloses a communications system in which a large number of endpoints communicate among one another in an orderly and protocol independent manner. The system is based on a short, fixed format packet which is switched among stations and within equipment in a contention-free manner without the use of general purpose processors. The system is distance independent, employs serial or parallel data paths, can use various media and can transport and switch data and digitized voice and video information in the same format and with the same equipment and transmission media. The effect of the system is to enable the construction of large metropolitan area networks which provide complete protocol conversion of all terminal types as well as transmission of data, voice, video and encrypted information.

The Giancarlo patent depicts several block diagrams and discloses the circuit for an integrated circuit implementation.

The Giancarlo patent fails to teach or disclose the specific claimed steps in claim 37 of loading a control register with control data to select a memory access controller, transferring and shifting a word of data in response to first control signals in respective first and second states, and transferring and shifting a word of data in response to memory access control signals while maintaining the first control signals in the second state.

Claim 37 is allowable.

Amended claim 25 now defines a method of reading words of data from a device coupled to a register, which is in series with a serial data output.

The method loads a controller with control data to provide read data control signals to the register and the device.

The method transfers a word of data in parallel from the device into the register in response to the control signals.

The method shifts data from the register in series to the serial data output in response to the control signals.

The method repeats the steps of transferring and shifting for additional words of data after the last data bit of the previous word of data is shifted out of the register without loading the controller with additional control data.

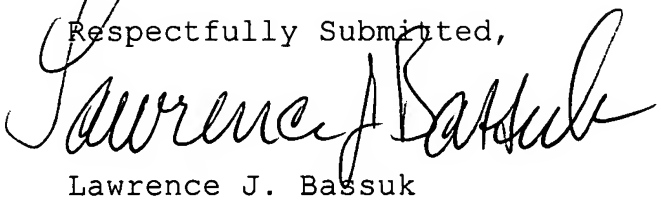
In contrast, both the Kyu and the Giancarlo patents fail to teach or disclose the specific claimed steps in claim 25 of loading a controller with control data, transferring and shifting a word of data in response to the control signals, and repeating the steps of transferring and shifting for additional words of data after the last data bit of the previous word of data is shifted out of the register without loading the controller with additional control data.

Claim 25 stands allowable.

The depending claims stand allowable for including further limitations not disclosed or suggested in the Kyu or Giancarlo patents.

The application is in allowable form and the claims distinguish over the cited references. Applicant respectfully requests reconsideration or further examination of this application.

Respectfully Submitted,



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